

Program: SE Information Technology Engineering

Curriculum Scheme: Revised 2012

Examination: Second Year Semester III

Course Code: SEITC304

Course Name: Analog and digital circuits

Time: 1 hour

Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	A certain inverting amplifier has a closed-loop voltage gain of 25. The Op-amp has an open-loop voltage gain of 100,000. If an Op-amp with an open-loop voltage gain of 200,000 is substituted in the arrangement, the closed-loop gain_____.
Option A:	doubles
Option B:	drops to 12.5
Option C:	remains at 25
Option D:	increases slightly
Q2.	If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?
Option A:	1
Option B:	2
Option C:	7
Option D:	8
Q3.	The format used to present the logic output for the various combinations of logic inputs to a gate is called a(n):
Option A:	Boolean constant
Option B:	Boolean variable
Option C:	truth table
Option D:	input logic function
Q4.	Which among the below stated boolean expressions do not obey De -Morgan's theorem ?
Option A:	$X+Y = X . Y$
Option B:	$X.Y = X + Y$
Option C:	$X.Y = X+Y$
Option D:	None of the above

Q5.	The boolean functions which can be represented by the sum of minterms and product of maxterms can be categorized in _____.
Option A:	standard form
Option B:	canonical form
Option C:	both a & b
Option D:	none of the above
Q6.	Which illustration from the below stated functions exhibits the conversion of product of maxterm form into sum of Minterm form if the value of product of Maxterm is $F(x,y,z) = \pi (6,8,10,11)$?
Option A:	$F(x,y,z) = \sum (7,9,12,13)$
Option B:	$F(x,y,z) = \pi (7,9,12,13)$
Option C:	$F(x,y,z) = \sigma (7,9,12,13)$
Option D:	$F(x,y,z) = S (7,9,12,13)$
Q7.	What are the OR terms present in product of sum form of the boolean expression called as ?
Option A:	minterms
Option B:	maxterms
Option C:	sum terms
Option D:	product terms
Q8.	It is possible to change the non-standard form of boolean function to a standard form by using _____.
Option A:	De-Morgan's Law / Theorem
Option B:	Duality Law / Theorem
Option C:	Complementary Law
Option D:	Distributive Law
Q9.	Which is the major functioning responsibility of the multiplexing combinational circuit?
Option A:	Decoding the binary information
Option B:	Generation of all minterms in an output function with OR-gate
Option C:	Generation of selected path between multiple sources and a single destination
Option D:	All of the above
Q10.	Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
Option A:	Data Selector
Option B:	Data Distributer
Option C:	Both a & b
Option D:	None of the above
Q11.	What does the small bubble on the output of the NANDgate logic symbol mean?
Option A:	open collector output

Option B:	tristate
Option C:	The output is inverted.
Option D:	none of the above
Q12.	Why do the D-flipflops receives its designation or nomenclature as 'Data Flipflops' ?
Option A:	Due to its capability to receive data from fliflop
Option B:	Due to its capability to store data in flipflop
Option C:	Due to its capability to transfer the data into flipflop
Option D:	All of the above
Q13.	The characteristic equation of D-flipflop implies that _____.
Option A:	the next state is dependent on previous state
Option B:	the next state is dependent on present state
Option C:	the next state is independent of previous state
Option D:	the next state is independent of present state
Q14.	What is the bit storage binary information capacity of any flipflop?
Option A:	1 bit
Option B:	2 bits
Option C:	16 bits
Option D:	infinite bits
Q15.	What is/are the directional mode/s of shifting the binary information in a shift register?
Option A:	Up-Down
Option B:	Left - Right
Option C:	Front - Back
Option D:	All of the above
Q16.	Match the following sequential Circuits with associated functions 1. Counter ----- A. Storage of Program & data in a digital computer 2. Register ----- B. Generation of timing variables to sequence the digital system operations 3. Memory ----- C. Design of Sequential Circuits
Option A:	1-A , 2-B , 3-C
Option B:	1-C , 2-B , 3-A
Option C:	1-C , 2-A , 3-B
Option D:	1-B , 2-C , 3-A

Q17.	A counter is fundamentally a _____ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it.
Option A:	register
Option B:	memory unit
Option C:	flipflop
Option D:	arithmetic logic unit
Q18.	Which property of unit distance counters has the potential to overcome the consequences of multi-bit change flashing that arises in almost all conventional binary and decimal counters?
Option A:	one bit change per unit change
Option B:	two bits change per unit change
Option C:	three bits change per unit change
Option D:	four bits change per unit change
Q19.	What contributes to the triggering of clock pulse inputs for all the flipflops excluding the first flipflop in a ripple counter?
Option A:	Incoming Pulses
Option B:	Output Transistion
Option C:	Double Clock Pulses
Option D:	All of the above
Q20.	What is the required relationship between number of flipflops and the timing signals in Johnson Counter?
Option A:	No. of flipflops = $1/2$ x No. of timing signals
Option B:	No. of flipflops = $2/3$ x No. of timings signals
Option C:	No. of flipflops = $3/4$ x No. of timing signals
Option D:	No. of flipflops = 4 x No. of timing signals
Q21.	One that is not the outcome of magnitude comparator is _____
Option A:	$a > b$
Option B:	$a - b$
Option C:	$a < b$
Option D:	$a = b$
Q22.	In a comparator, if we get input as $A > B$ then the output will be _____.
Option A:	1
Option B:	0
Option C:	A
Option D:	B
Q23.	Comparators are used in _____.
Option A:	Memory
Option B:	CPU

Option C:	Motherboard
Option D:	Hard drive
Q24.	The other name for Gain is _____
Option A:	Scaling factor
Option B:	Output
Option C:	Amplifying factor
Option D:	Scaling level
Q25.	The common-mode voltage gain is
Option A:	smaller than differential voltage gain
Option B:	equal to differential voltage gain
Option C:	greater than differential voltage gain
Option D:	none of the above